

Name: _____ Date: _____

Fill in the output column “S” for each of the logic gates circuits.

1)

```
graph LR; A --> AND1[AND]; B --> AND1; AND1 --> NOT1[NOT]; NOT1 --> S
```

A	B	S
0	0	
0	1	
1	0	
1	1	

2)

```
graph LR; A --> OR1[OR]; B --> OR1; OR1 --> NOT1[NOT]; NOT1 --> S
```

A	B	S
0	0	
0	1	
1	0	
1	1	

3)

```
graph LR; A --> OR1[OR]; B --> NOT1[NOT]; NOT1 --> OR1; OR1 --> S
```

A	B	S
0	0	
0	1	
1	0	
1	1	

4)

```
graph LR; A --> NOT1[NOT]; NOT1 --> AND1[AND]; B --> AND1; AND1 --> S
```

A	B	S
0	0	
0	1	
1	0	
1	1	

5)

```
graph LR; A --> AND1[AND]; B --> AND1; AND1 --> OR1[OR]; C --> OR1; OR1 --> S
```

A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

6)

```
graph LR; B --> OR1[OR]; C --> OR1; OR1 --> AND1[AND]; A --> AND1; AND1 --> S
```

A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

7)

```
graph LR; A --> OR1[OR]; B --> OR1; OR1 --> OR2[OR]; C --> OR2; OR2 --> S
```

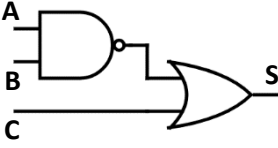
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8)

```
graph LR; B --> AND1[AND]; C --> AND1; AND1 --> OR1[OR]; A --> OR1; OR1 --> S
```

A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

9)



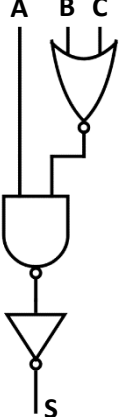
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

10)



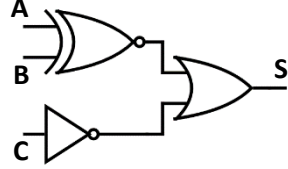
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

11)



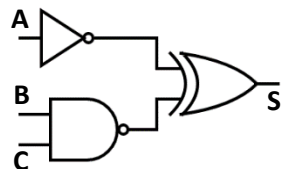
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

12)



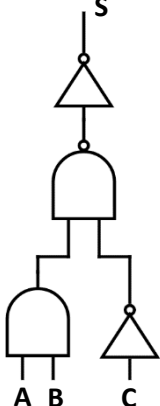
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

13)



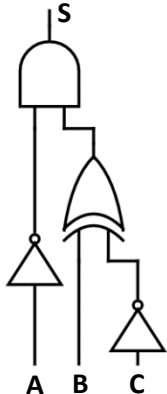
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

14)



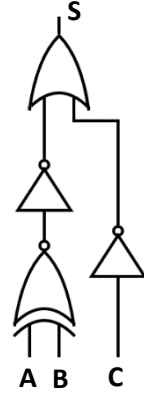
A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

15)



A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

16)



A	B	C	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	